REMARKS

Claims 1-31 are pending in the application

Claims 1-31 have been rejected.

Claims 9 and 20 have been amended.

Claims 11 and 22 have been cancelled.

Objections to the Specification

The Office Action objects to informalities to a parenthetical in p.11, ll.14-15 (Application, ¶ [0035]). Applicants have amended ¶ [0035] to delete the objected-to parenthetical. Applicants respectfully submit that this amendment renders the objection moot.

The Office Action objects to text describing the relationship between the described "hysteresis factor" and "evaluation time period" as seeming "over-complicated or not explained well." *See* Office Action, p.2. Specifically, the Office Action states:

> Paragraph 0039 indicates that an "evaluation time period" is equal to or approximates the "hysteresis factor" divided by the product of the "alarm set threshold" and the transmission "bit rate," while paragraph 0040 indicates that once the "evaluation time period" is determined, it is used "to determine and scale" the "alarm set threshold" and the "alarm clear threshold," which seems over-complicated or not explained well.

Office Action, p.2. Applicants respectfully submit that the expressed confusion may be due to misinterpreting the cited paragraphs. Specifically, Paragraph [0040] states:

> Once the evaluation time period exponent is determined, it is used to determine and scale as necessary the physical link error alarm set threshold and physical link error alarm clear threshold.

Application, ¶ [0040] (emphasis added). Thus, it is the evaluation time period exponent that is used for the described determining and scaling, not the evaluation time period itself, as suggested by the Office Action. Further, derivation of the evaluation time period exponent is disclosed in the previous paragraph:

> According to one embodiment of the present invention, the exponent of the evaluation time period is determined and used in place of the actual evaluation time period to avoid the use of floating point operations. In the described embodiment, the evaluation time period exponent is calculated as the difference between the exponent of the link error alarm set threshold and the exponent of the compensated transmission bit rate parameter (i.e., the difference between the bit-rate adjustment factor and the integer between 0 and 2 used to express the transmission bit rate).

Application, ¶ [0039]. Applicants hope that this explanation is useful in clearing up any confusion created by these paragraphs that use very similar language to describe different variables.

Objections to the Drawings

The Office Action objects to the drawings under 37 CFR § 1.83(a) and indicates that the drawings do not reflect the limitations of dependent Claims 11 and 22. As indicated above, Applicants have canceled Claims 11 and 22. Applicants note that the cancellation of these claims is performed for the sake of progressing prosecution and is not intended as concession of the substance of the objections raised to the drawings. Applicants further reserve the right to argue the substance of the objections at a later time.

In light of the cancellation of these claims, Applicants respectfully submit that the objections to the drawings have been rendered moot.

Rejection of Claims Under 35 U.S.C. §112

Claims 9, 11, 20 and 22 are rejected under 35 U.S.C. §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

In response to this rejection, Applicants have amended Claims 9 and 20 to clarify the subject matter of those claims. Applicants respectfully submit that support for these amendments can be found at least in ¶¶ [0035] – [0041] of the present Application. In addition, Applicants have canceled Claims 11 and 22. In light of these amendments and cancellations, Applicants respectfully submit that the rejections of these claims under 35 U.S.C. § 112 have been rendered moot.

Rejection of Claims Under 35 U.S.C. §102

Rejections under Brief Reference

Claims 1-3, 6-8, 10, 12-14, 17-19, 21, 23-26 and 29-31 are rejected under 35 U.S.C. §102(b) as being anticipated by U.S. Patent No. 5,459,731 issued to Brief et al. ("Brief"). Applicants respectfully traverse this rejection.

Claims 1, 12 and 23: Independent Claims 1, 12 and 23 each contain limitations of substantially the following form:

> determining an operational link error rate of a link; and
>
> estimating a real-time physical link error rate of said link using said operational link error rate.

See, e.g., Claim 1. Applicants respectfully submit that the cited sections of Brief fail to provide disclosure of these claim limitations.

Applicants submit that the sections of Brief cited by the Office Action and purportedly disclosing the above limitations do not provide for estimating a real-time physical link error rate using a determined operational link error rate. The section of Brief cited by the Office Action for the "determining" limitations provides only that, in certain situations, the disclosed controller purportedly responsible for detecting link errors does not detect each error.

> In some embodiments, controller 120 does not detect all errors, and thus the actual LER can be higher than computer [sic] by controller 120. For example, in some FDDI embodiments, controller 120 detects only the following errors. In the ALS or CLS line states, a violation symbol is detected in the upper or lower nibble. In the ILS state, an error is detected if a symbol in either nibble is not Q, H or I and if successive nibbles do not for JK (the starting delimiter).

Brief 4:22-29 (cited at Office Action, p.5) (emphasis added). This cited section provides no disclosure of determining an error rate of a link, but only relates to deficiencies in detecting individual errors.

Brief does provide disclosure of calculating a link error rate (LER) by using a weighted average time interval between link errors, wherein the highest weight is given to the most recent time interval between errors. *See* Brief 3:67-4:20. Thus, using the information disclosed in Brief 4:22-29, an LER estimate can be calculated. The Office Action implies that this LER corresponds to the claimed operational link error rate. But the Office Action provides no reference to disclosure in Brief that supports a proposition that this LER is then used to (or could even be used) estimate a "real-time physical link error rate," as claimed. The Office Action only suggests that "[t]he FDDI standard specifies a maximum link error rate (LER) of 2.5×10^{-10} bits (column 3, lines 52-56), which serves as an 'alarm set threshold' for a 'real-time physical link error rate.'" Office

Action, p.5. But neither this portion of the Office Action, nor the cited text, provides for using the above-discussed LER in order to estimate or determine the suggested "real-time physical link error rate." Instead, Bridge uses the above-discussed LER (suggested by the Office Action to be the operational LER) directly for Bridge's purposes.

Applicants further submit that one would not expect Brief to provide disclosure of the claimed "determining" and "estimating." The purpose of Brief is to relieve a microprocessor of the task of calculating a link error rate and comparing that link error rate to a threshold. *See* Brief 1:38-59. Brief purports to accomplish this by performing link error rate computation and comparison at the physical layer. *See* Brief 1:65-67. A link error monitor (LEM) is provided with threshold registers and circuitry for continuously monitoring the link error rate. *See* Brief 3:37-43. The LEM then purportedly computes the LER by taking a weighted average of time intervals between error bits. *See* Brief 3:57-4:6. This link error rate is disclosed to be compared with the set thresholds. *See, e.g.*, Brief 3:40-42. Thus, Brief discloses directly calculating a link error rate from the disclosed time intervals and comparing that with the set thresholds to determine whether to interrupt the microprocessor. Brief is not concerned with, nor does Brief contemplate, any computation of a "real-time physical link error rate" using the calculated link error rate, nor would Brief have any use for such a different link error rate.

For at least these reasons, Applicants respectfully submit that Brief fails to provide disclosure of each limitation of independent Claims 1, 12 and 23, and all claims depending therefrom, and cannot be said to anticipate these claims. Applicants therefore respectfully request the Examiner's reconsideration and withdrawal of the rejections to these claims and an indication of the allowability of same.

Rejections under Burke Reference

The Office Action rejects Claims 1-8, 10, 12-19 and 23-31 under 35 U.S.C. § 102(b) as purportedly being anticipated by U.S. Patent No. 6,310,911 issued to Burke et al. ("Burke"). Applicants respectfully traverse these rejections.

Claims 1, 12 and 23: Regarding independent Claims 1, 12 and 23, the Office Action cites generally to the entire Burke patent without any citation to any specific portion of Burke for the proposition that Burke anticipates these claims. Applicants respectfully submit that the particular parts of Burke that are relied upon in the Office Action have not been designated as nearly as practicable, and the pertinence of each reference has not been clearly explained, both as required by 37 C.F.R. §1.104(c)(2). Applicants respectfully request that the Examiner provide specific citation to those sections of Burke that the Examiner posits provides disclosure of the claimed limitations. Nevertheless, Applicants have made every effort to respond to the rejections outlined in the Office Action.

As an initial matter, after a search of Burke's text, Applicants note that Burke provides no disclosure, either explicit or implicit, of a "real-time physical link error rate" or estimating such a physical link error rate from an operational link error rate. Burke purports to be concerned with calculating a Bit Error Ratio and comparing that Bit Error Ratio with set thresholds. *See* Burke 3:17-30. The Office Action appears to suggest that the disclosed thresholds correspond to the claimed "real-time physical link error rate." Office Action, p.6. But Applicants have found no disclosure that these thresholds are estimated using an operational link error rate, as claimed.

The Office Action also suggests that Burke's Bit Interleaved Parity (BIP) errors correspond to the claimed operational link error rate. But Burke discloses a BIP not as a link error rate, but instead as an indication that an error occurred in a frame. *See* Burke 9:1-2. Burke then discloses that BIPs are purportedly used to calculate a Bit Error Ratio (Burke 9:1-10:15) and BIPs are accumulated over time to acquire better confidence in the calculated Bit Error Ratio (Burke 10:16-19). It is this accumulated Bit Error Ratio that is provided to Burke's monitor for comparison with the set thresholds. There is no disclosure of using the Bit Error Ratio or the BIPs to calculate the claimed "physical link error rate."

Applicants further submit that it would make no sense, in the context of Burke, to estimate the thresholds (which the Office Action corresponds to the claimed "real-time physical link error rate") from the BIP errors (which the Office Action corresponds to the claimed "operational link error rate") since Burke discloses comparing the Bit Error Ratio (which is calculated from the BIPs) against the thresholds. Burke provides no indication that it would be desirable to adjust the thresholds in accord with the measured BIPs, and the Office Action provides no indication of why it would be desirable to do so.

For at least these reasons, Applicants respectfully submit that Burke fails to disclose all of the limitations of independent Claims 1, 12 and 23, and all claims depending therefrom, and those claims are in condition for allowance. Applicants therefore respectfully request the Examiner's reconsideration and withdrawal of the rejections to these claims and an indication of the allowability of same.

CONCLUSION

In view of the amendments and remarks set forth herein, the application and the claims therein are believed to be in condition for allowance without any further examination and a notice to that effect is solicited. Nonetheless, should any issues remain that might be subject to resolution through a telephonic interview, the Examiner is invited to telephone the undersigned at 512-439-5090.

I hereby certify that this correspondence is being deposited with the United States Postal Service as First Class Mail in an envelope addressed to: Mail Stop Amendment, COMMISSIONER FOR PATENTS, P. O. Box 1450, Alexandria, VA 22313-1450, on December 19, 2006.

Attorney for Applicant(s) — Date of Signature: 12/19/2006

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